Key Metrics and Reliability Prospects for High Performance PRAM

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ABSTRACT

This paper reviews the key issues of associated with high performance and high density phase change random access memory (PRAM) as a promising candidate for universal memory device. A universal memory requires properties of high read/write performance and superior reliabilities. However, it is restricted by peculiar properties of phase change memory cell such as trade-off relation between speed and data retention, cycling endurance failure by phase segregation and thermal disturbance. In this paper, several suggestions to overcome the reliability issues are introduced with recent experimental results.

Key words: PRAM, RESET Current, tSET, Reliability, Endurance, Retention, Thermal Disturbance

1. INTRODUCTION

Phase change random access memory (PRAM) has been widely investigated as not only non-volatile memory but also high performance Storage Class Memory (SCM) including hybrid managed memory devices. New class of solid state memory as storage class memory or hybrid type memory requires higher data rate and more robust reliability aspect ad described table 1. In this paper, we describe the key reliability issues for high performance PRAM and suggest the several solutions to mitigate the bottle neck in future application of PRAM.

Table 1. Target specification comparison between SCM and conventional NVM application [1][2]

Item	*SCM*	*NVM (NOR, NAND)*
Access time	50~1,000 ns	70~100 ns, 15~50 us
Data rate	100 MB/s	0.5~2 MB/s, 10+ MB/s
Endurance	10^9~10^{12}	10^4~10^5
Retention	10 years	10 years
Thermal disturbance	10^9~10^{12}	10^4~10^5

2. RESET CURRENT SCALING

RESET current reduction is one of the key issues for high data rate in high performance PRAM. Two approaches have been developed to reduce the RESET current. One is to increase the resistance of heating elements by contact dimension scaling or resistivity increasing. The other is to improve heat efficiency by reducing a required programming volume. In order to dramatic decrease of RESET current, combination of two approaches are essential. RESET current decreases by about over 50% in the confined cell with small high resistive electrode [3].

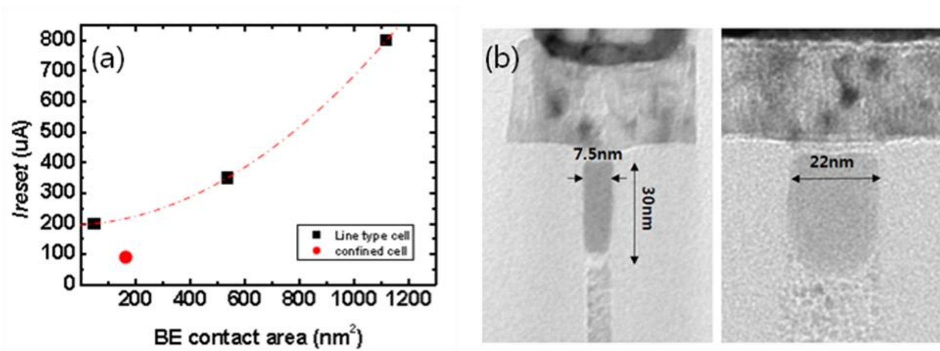

Fig. 1 (a) RESET current scaling of line type cell and confined cell as a function of contact area (b) Dash type confined cell structure.

3. GST INTEGRITY

GST integrity means thin film quality of phase change material. GST is seriously affected by deposition and post etching process. Especially, voiding induced by Ar incorporation or chemical damage give rise the SET failure. GST integrity can be improved through the deposition process control to increase the film density and integration scheme to avoid the etching process. Ellipsometry methodology is introduced to analyze the density of GST film indirectly which is closely linked to void in GST thin film. Furthermore, void simulation was utilized for void expectations. A long wave optical pulse used to measure the n, k value due to its low transmittance into GST film and computational algorism is applied to analyze the portion of void in GST film [4].

4. ENDURANCE

Endurance failures are classified into four groups which are the stuck to high resistance of set state (the stuck RESET), the stuck to low resistance of RESET state (the stuck SET), SET tail and RESET tail away the failure criteria from the SET or RESET distribution. Stuck RESET and SET tail are caused by the void generation inside the programming volume and stuck SET and RESET tail are owing to the compositional change. Both voiding and compositional changes are affected from the bias dependent atomic transport due to electro-migration in the molten GST and/or incongruent melting occurred at the boundary region of liquid and solid phases [5][6]. Isolated confined cell can inhibit the endurance failure by reducing the atomic transport reservoir and boundary region between liquid and solid. Fully confined cell shows over 10^{12} endurance cycles of writing operations. And also, endurance failure as a function of programming energy guaranteed up to 10^{15} cycles [7].

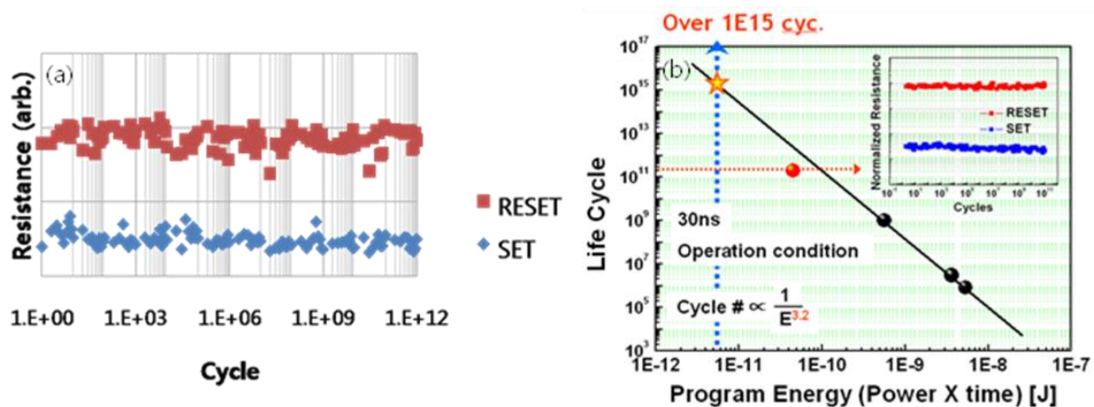

Fig. 2 (a) Endurance characteristics for dash type confined cell. There is no failure during 10^{12} cycles of write operations. (b) Cycled failure as a functiona of programming energy guaranteed up to 10^{15} cycles.

5. tSET vs. RETENTION

One of the main demands of high performance PRAM is high write speed property with superior data retention. However, it is restricted by peculiar properties of phase change materials such as trade-off relation between crystallization time and data retention because their origin is the same. Long-term data loss at operation temperature in PRAM is explained by nucleation and growth kinetics of phase change material and the percolation theory in an amorphous matrix. Many researchers have suggested the fast crystallized phase change materials and high Tx (Crystallization temperature) materials respectively. However it is hard to combine the high speed and high retention property as mentioned above. SbTe or doped GeTe based material in confined cell structure shows fast crystallization speed under several tenths of nano second with excellent data retention property retaining data for over 10 years at 85℃. In our case, a very confined dimension seems to makes nucleation probability decrease, and lead good data retention with high speed [8].

6. THERMAL DISTURBANCE

Thermal disturbance occurs at the nearest amorphized cell which is thermally crystallized by high temperature during programming the selected cell. Therefore it is closely related to the retention property of phase change material and thermal diffusion between nearest cells. In general, Thermal disturb is observed at line type GST cell. However, isolating a cell by dielectric materials such as oxide or silicon nitride is helpful to improve the thermal disturbance property [9][10].

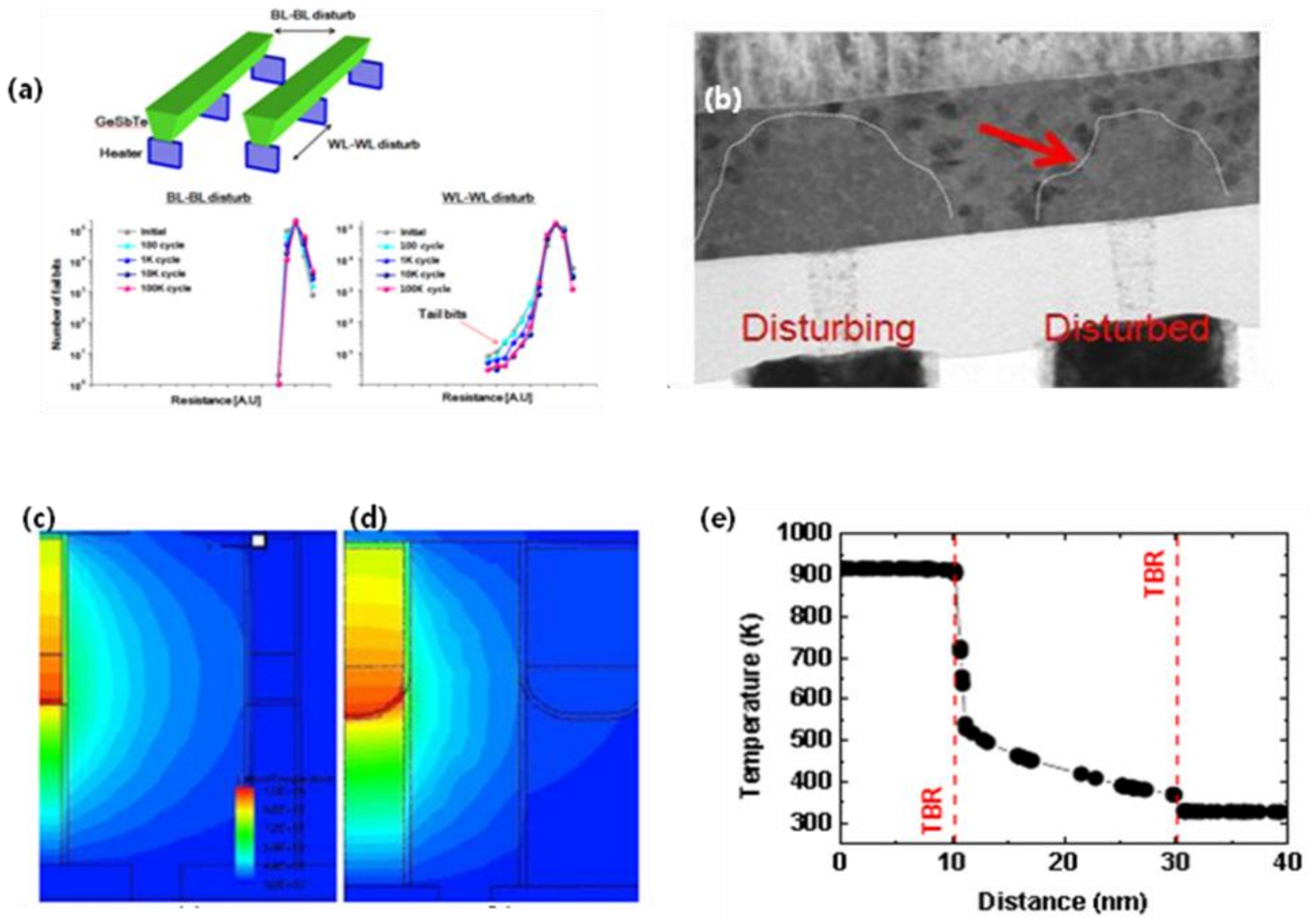

Fig. 3 (a) RESET resistance distribution of the nearest cell according to the number of the programming cycles (b) Cross - sectional TEM micrograph of thermally disturbed cell (c) Temperature profile of dash type confined cell along with WL direction and (d, e) BL direction. Temperature discontinuity occurs at interface due to thermal boundary resistance.

7. CONCLUSION

The key metrics and possible solutions for future high performance PRAM have been discussed. Current features of NVM based PRAM is insufficient to satisfy the SCM like high performance PRAM device. Improvement of GST integrity, RESET current, speed, endurance, retention and thermal disturbance properties is a critical prerequisite for future high-end applications. In this paper, we have been suggested the introduction of isolated confined cell structure with new phase change material could be a key to opening up the SCM and/or hybrid application possibilities for the PRAM.

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Biographies

Dr. Dongho Ahn was born in 1968. He received a B.E and M.E in electronics from Konkuk and Kyung-Hee University, Seoul, Korea, respectively. And he received a Ph.D. degree in Materials Science and Engineering with a thesis on phase change material and devices from Seoul National University, Seoul, Korea. He has been a principal engineer at Samsung Electronics since 1992. His research area has been chalcogenide and electrode material for phase change memory, process engineering and reliability.