Scalability of thermal phase-change storage and memory

Hendrik F. Hamann*, Levente J. Klein
IBM T.J. Watson Research Center,
1101 Kitchawan Road ,Yorktown Heights, NY, 10598, USA
hendrikh@us.ibm.com

In this work we discuss relevant aspects of the scaling physics of thermal information storage on phase-change (PC) materials. First, we review prior experiments, where a heated AFM tip was implemented as an ultra-small heat source to demonstrate erasable PC bit patterns at a density of up to 3.3 Tb./in.^{2}. Second, properties of thin-film, resistive nanoheaters with dimensions of less than 30 nm are investigated, which could be a technically-viable alternative to the AFM-based approach. Third, an all-thermal storage / memory concept is discussed, where a single heater patterned on a PC material, writes, erases and reads the PC storage media. Finally, we show experimental data indicating strong sub-continuum effects in Silicon (Si) below 300 nm and discuss the impact for PC thermal recording.

I. Introduction:

One of the most important features of a new technology can be its "scalability". Scalability provides a way to recoup the (possibly) large initial investment for the development of this technology by "simply" scaling the initial technology to provide better performing products at lower cost at each scale. Good examples for this are semiconductor chips and hard disk drives, where impressing technology improvements were accomplished by repeatedly scaling a base technology. As PC storage and memory has been continuously making inroads, in particular in the area of non-volatile memories, the question of ultimate physical limitations and scalability is attracting more and more interest.

Besides many technical and engineering challenges in the realization of ultra-dense PC storage and memory, many aspects of thermal recording physics and nanometer scale mechanisms behind the PC process are not completely understood [1-5]. For example it is not clear how melting and crystallization kinetics is influenced by the bit size or whether the limited numbers of nucleation sites at small dimensions impact the nanoscale bit formation. The crystallization involves the stochastic process of nucleation and growth. It is believed that the nucleation is heterogeneous starting with a critical nucleus, which can be a function of many variables including the temperature and the competition between surface tension and the free-energy difference between amorphous and crystalline states.

Besides many open questions regarding the nanoscale recording mechanism, fundamentals of the actual heat generation, heat conduction and transfer are not understood as well, especially as PC technologies are being scaled. For example, many non-volatile PC memory designs involve Si as a main heat carrier. However, the average mean free path (Λ) of heat carrying phonons in Si is approximately 300 nm at room temperature, which can impact the heat transfer. Specifically, the small dimensions will result into significant boundary scattering reducing the heat transfer through thin layers of Si (as used in SOI). Because the actual hotspot dimensions are smaller than the mean free path, the heat transfer in the vicinity of these hotspots is below the continuum assumption and thus "ballistic", which will result into an additional thermal resistance in comparison to what one would expect based on simple Fourier heat conduction. Furthermore, doped Si has pronounced thermoelectric effects which can change the heat generation distribution significantly. Finally, because a PC memory / storage technology utilizes very thin films, interface resistances between the different layers will play a major role in the actual heat transfer, which in turn determines important scalability properties such as adjacent bit heating.

II. AFM-based thermal recording experiments

In this work we investigate some important aspects as they relate to the scalability of the thermal PC recording process. In order to separate the thermal writing process from other electric field induced film modifications we use "indirect" heating to alter the phase of the material. This approach is different from most previous investigations, which are based on current induced (or threshold switching), where the PC material is directly Joule heated while undergoing a very strong non-linear resistance change. The indirect heating concept has the advantage that the electrical impedance of the heater can be controlled independently from the PC material and thus provides excellent control during the sensitive write/erase process.

We start with reviewing some recent work [1] where a heated atomic force microscope (AFM) tip was used to demonstrate very dense PC bit patterns. The experimental setup is illustrated in Fig.1. A diode laser was focused on the back of an AFM cantilever thereby heating the AFM tip, which acts as *ultra small* heat source (dimensions of ~5-10 nm). The sample is a standard $Ge_2Sb_2Te_5$ (GST) film (18 nm film thickness) deposited on an cleaved mica substrate via RF sputtering from a stoichiometric target. The crystallization temperature was measured on a hotplate (~185^{o}C). Before starting the recording experiments the film was "cycled" back and forth a couple of times using a laser diode.

As illustrated in Fig.1 the heated AFM tip is approached to GST film and writes crystalline bits into an amorphous film. The distance control of the AFM is accomplished using a heterodyne interferometer (not shown here). Because the crystalline phase has a higher mass density, the actual bits appear as small valleys in the subsequent AFM scans. The actual height difference (~7 A^{o} out of 180 A^{o}) matches the expected density difference between the two phases. We note that the AFM tip is retracted several nanometers before applying the laser pulse. In every experiment the optimum retraction distance and laser power was determined by running a set of experiments with the goal to obtain the smallest bits. The actual mechanism of heat transfer between the tip and film is discussed further below. As reported in Ref.[1] the approach depicted in Fig.1 led quite readily to erasable bit patterns at a density of up to 3.3 Tb./in.^{2} with an average distance of only 14 nm between the bits and bit sizes of ~ 8 nm. Even at these high storage densities we had evidence that further improvements might be just a matter of optimization. By studying different film thicknesses (18, 24, 30 nm) as well as using different AFM tips (sizes: ~5,~10,~15 nm (made by ion milling)) we found evidence that the bit size may be just governed by the thermal gradient rather material properties. Clearly, this could be improved by "sharper" AFM tips, thinner PC films and higher thermal conductivity substrates.

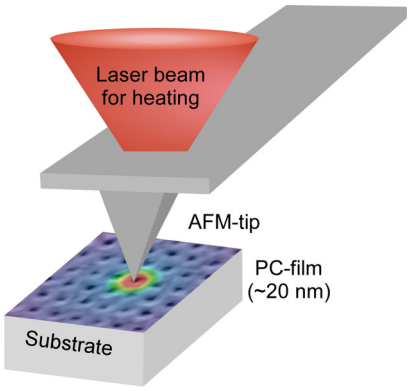

Fig.1: Experimental Setup

II. Nanoheater properties and heat transfer

While the AFM experiments were useful to understand whether thermal writing can generate sub 10 nm bits, we subsequently replaced the AFM tips with small thin film resistors (or nanoheaters) as a possibly more practical implementation for generating small hotspots. For this purpose we have fabricated a series of 4-wire, thin film (30 nm) nanoheaters with dimensions down to 20 nm on a Si/SiO2 substrate using state-of-the-art e-beam lithography (see Fig.2). The nanoheaters were carefully characterized by measuring the resistance change as a function of power using a 4-wire electrical setup. In combination with the (measured) temperature coefficient of resistance (TCR) we determined the (resistance weighted average) temperature of the nanoheater as a function of dissipated power (e.g., thermal resistances ~ 1 K/μW). Because of annealing effects, the "cold" resistance (i.e., at low power) as well as the TCR could change during the experiments. However, we established that the actual thermal resistance remains constant. Specifically, we annealed the nanoheater for an extended period at a constant power and then re-measured (from time to time) the cold resistance, TCR and the IV characteristics. In

all cases (i.e., different nanoheater materials (Pt, NiCr, Cr, W) and film thicknesses etc.) a constant thermal resistance was found (within +/- 5 %).

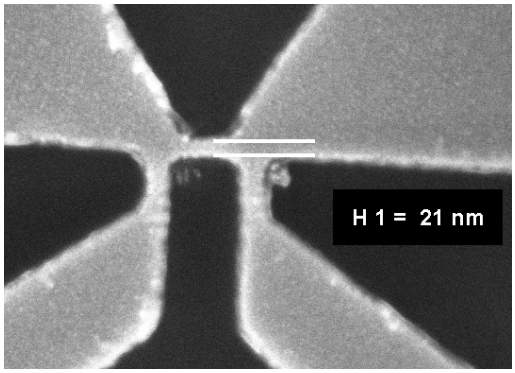

Fig.2: SEM of nanoheater

The nanoheaters have multiple purposes in the experiments. While the nanoheater technology may be a more viable solution for generating small hotspots and thus open up the possibility for commercially interesting applications, they can also be used as small temperature probes for understanding nanoscale heat transfer. Towards that end we first scanned a powered-up nanoheater with a "cold" AFM tip. In this case, heat is transferred from the nanoheater to the cold AFM tip while the change in resistance or temperature of the nanoheater is monitored. As demonstrated in Ref.[1] the heat is very much defined to the heater dimensions, which is consistent with the measured thermal resistance as well as detailed finite element (FE) modeling results.

We also measured the distance dependence of the heat transfer through the gap between the nanoheater and the AFM tip (see Fig.3). In combination with thermal resistance and the temperature change the power transferred through the "gap" is determined as a function of tip to nanoheater distance. During the approach the AC-vibration as well as the DC-deflection signal of the AFM lever is monitored. Both signals can be used to infer the distance from the surface. For the AC-vibration the actual dithering amplitude was reduced to 4 A^{o}_{pp}. Fig.3 shows two important results: First of all, *before* the DC-deflection signal of the lever indicates "hard" contact with the nanoheater surface, a substantial heat transfer can be observed. Specifically, 1 μW of power is transferred from the heater to the 5 nm radius tip at a distance of 2 nm (away from the hard contact point) and a temperature differential of ~200 K (neglecting additional thermal resistances within the AFM tip). This power flow corresponds to a heat flux of up to ~ 200 MW/m^2 K. FE modeling shows that such heat flux is certainly sufficient to switch PC materials back and forth. Consequently, assuming that similar heat fluxes can be accomplished using a "flying" head coupled to a disk with a PC film via an air-bearing surface, it might be feasible to use a nanoheater for PC recording similar to magnetic recording in hard disk drives. Second, taking the AC-vibration signal in Fig.3 into account it is evident that the AC vibration is significantly damped before the hard contact point indicating a "very soft" contact layer between the tip and surface. In essence, the data of Fig.3 suggest that a very soft layer between tip and nanoheater is responsible for the heat transfer allowing the PC film to be thermally switched. Extensive heating of the nanoheater did not cause this layer to evaporate. The explanation of a conduction path via a soft contact layer is consistent with the observations that both the distance dependence of the heat transfer between tip and nanoheater as well as temperature dependence of this heat flow is approximately linear.

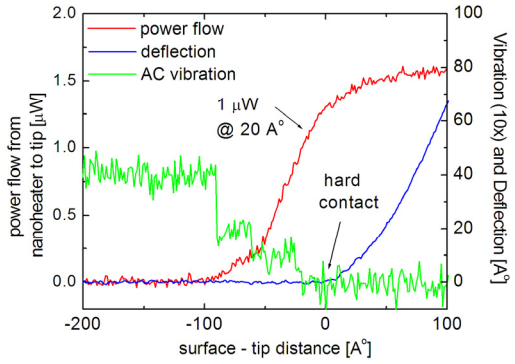

Fig.3: AFM approach curve.

III. Nanoheater Phase Change Recording

In the next set of experiments of Ref.[1] we patterned nanoheaters directly onto a GST films (here 40 nm thickness), which were sputtered on Si/SiO2 (20 nm) substrate. For writing (amorphization) and erasing (crystallization) a 30 and 100 ns heat pulse is applied to the ~40 Ohm nanoheater, respectively. For reading we use the nanoheater as a temperature probe exploiting the difference in thermal conduction between the amorphous and crystalline phase [6].

By heating the nanoheater only moderately (so no crystallization or amorphization occurs) and monitoring the electrical resistance for a given current, the phase of the GST film can inferred. A high electrical resistance shows an amorphous phase below the nanoheater (low thermal conductivity) while a lower electrical resistance indicates a crystalline phase (higher thermal conductivity). In Ref.[1] we showed that this all-thermal memory cell (which consists of a single thin film nanoheater/resistor) can read/write and erase repeatedly. While the temperature difference between the two phases at a moderate reading current was ~ 50 %, the actual electrical resistance change in the nanoheater was 6 %.

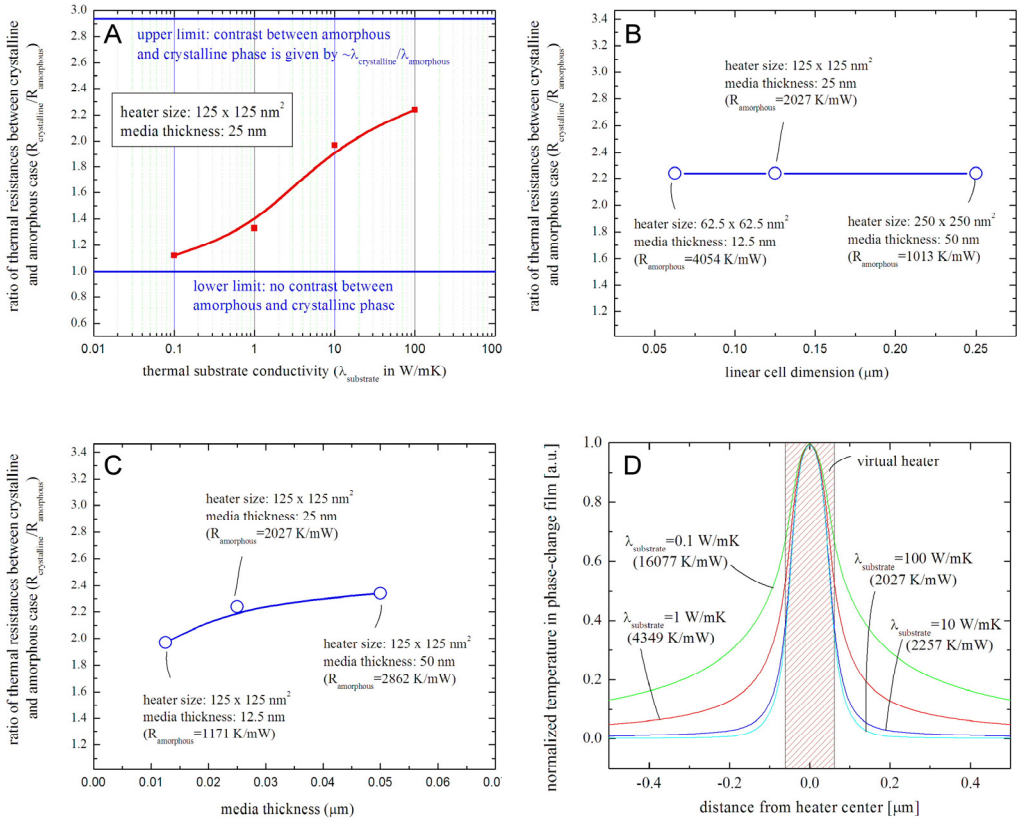

Fig.4: Ratio of thermal resistances for both phases as a function of substrate thermal conductivity (A), linear cell dimensions (B) and media thickness (C). Temperature distributions for various cell designs (D) (see text for details)

Before discussing sub-continuum heat conduction effects and how this might affect thermal PC recording we use here a FE thermal model to understand some of the "classical" scaling physics of such memory cell. Clearly, one of the technical challenges is to increase the read contrast ratio, which is governed by the ratio of the thermal resistances between the amorphous and crystalline phase. In these calculations the heater size is 125 x 125 nm^2 and the thermal conductivity of the amorphous and crystalline form is assumed to be ~0.17 W/mK and ~0.5 W/mK, respectively [6]. Here we have calculated the thermal resistances of this memory cell for the case of an amorphous ($R_{amorphous}$) and crystalline ($R_{crystalline}$) phase beneath the nanoheater. The phase outside of the nanoheater is assumed to be crystalline. Fig.4 A-C shows the ratio these two thermal resistances ($R_{amorphous}$ / $R_{crystalline}$) as a function of substrate thermal conductivity, linear cell dimensions and PC film thickness, respectively. Fig.4D shows the resulting temperature profiles for the various cases. Most interesting, Fig.4B shows a constant ratio as function cell size showing scalability of the thermal PC approach (at least from a classical view point).

Table 1 shows calculated operating conditions for this exemplary 125 x 125 nm^2 memory cell on a silicon substrate ($\lambda_{substrate}$ ~ 100 W/mK) with a 20 nm PC film. We assume a 30 Ω square heater with a TCR of α=0.3 % K^{-1} (e.g., Platinum). In these simple estimations we neglect changes of the thermal resistances during the write/erase process. The ambient temperature is assumed to be 20°C. The resulting temperatures as a function of applied current can be simply estimated by:

$$T = \frac{R_o I \cdot R_{amorphous\,/\,crystalline}}{1 - \alpha R_o I \cdot R_{amorphous\,/\,crystalline}}$$

Table 1 demonstrates that we can expect a read contrast ratio between amorphous and crystalline bit of ~ 25% with a constant current of 1.3 mA. The heater temperatures are 167°C and 73°C for the amorphous and crystalline phase, respectively. This corresponds to heater resistances of 43.1 Ω and 34.8 Ω during the reading process, respectively. The heater temperatures during reading are low enough and do not alter or degrade the phase of the recording media. While the data in Table 1 is just an illustrative example it is easy to play with the model to envision more optimized solutions.

operation	Heater temperature [°C]	heater resistance [Ω]	power in heater [mW]	thermal resistance [K/mW]	heater current [mA]	heater voltage [mV]
standby	20	30	-	-	-	-
Write	520	75	0.556	900	2.72	204
Erase	320	57	0.150	2000	1.62	92
read amorphous bit	167	43.1	0.073	2000	1.3	56
read crystalline bit	73	34.8	0.059	900	1.3	45

Table 1: Operating conditions of an all-thermal PC memory cell (see text for details).

IV. Sub-continuum heat conduction effects

It is interesting to investigate the impact of sub-continuum heat conduction effects on the thermal PC recording process. Most PC memory cells involve Si as a major heat carrier. While boundary scattering effects in thin layers of Si have been experimentally investigated [7], there is a significant lack of experimental data on ballistic heat conduction effects in Si [8]. The reason for this is related to the difficulties to control the boundary resistances for very small heat spots, where these effects would be most evident. Here we present some experimental data where two nanoheaters (30 nm) are placed in close vicinity directly on a Si substrate. The first device acts as a heater/sensor and the second just as a sensor (i.e., low current to avoid any heating). Specifically, we measured the ratio between the heater (T_H) and the sensor temperature (T_S) for different distances, different heater/sensor sizes and Si substrate temperatures. The different substrate temperature allows tuning the phonon mean free path (Λ) from 300 nm at 300 K up to above 50 μm at 30 K [9]. In Fig.5 we have normalized the distance between the heaters to the size (i.e. width of heater) of the heat source. The different data points show the measurements for a given τ, which is given by the ratio of the heater size to the mean free path of the phonons. In essence, Fig.5 shows the resulting

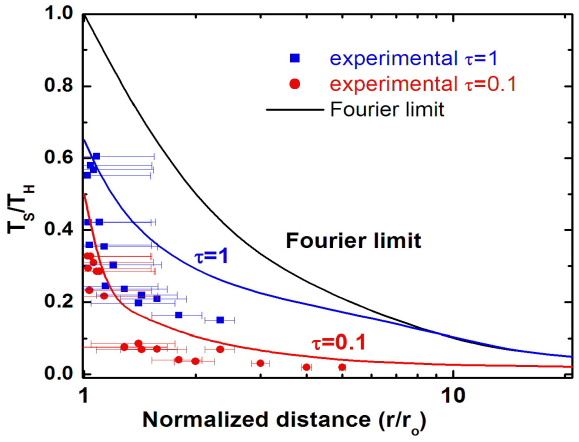

Fig.5: Temperature gradients for nanoheater for different τ (i.e., size of heater / phonon mean free path) (see text for details).

temperature *gradients* for different heater sizes (normalized by the respective mean free path of the phonons). For reference we have plotted the Fourier limit as well as results from BTE (Boltzmann-Transport Equation) simulations (solid lines) [8]. The data in Fig.5 shows significantly enhanced thermal gradients at smaller length scales, which is due to a combination of ballistic (sub-continuum) heat conduction and increased boundary resistances at small scales. The details are discussed elsewhere [10].

V. Conclusion:

In conclusion we have reviewed some relevant aspects of the "scaling" physics of thermal storage on PC (PC) materials. Although classical concepts suggest scalable memory and storage solutions, the impact of nanoscale and sub-continuum effects may play a very important role.

Acknowledgement: The authors acknowledge contributions from M. Asheghi, K. Etessam-Yazdani, H. J. Ryu, Y. Martin, H.K. Wickramasinghe, M. Rooks, and M.P. O'Boyle.

V. References:

[1] H.F. Hamann, M. O'Boyle, Y.C. Martin, M. Rooks, H.K. Wickramasinghe, Nature Mat. **5**, 383 (2006).

[2] A.L. Greer, 2005 European Symposium on Phase Change and Ovonic Science; available at http://www.epcos.org/pdf_2005/Greer.pdf.

[3] K. Sugawara, T. Gotoh, K. Tanaka, *J. Appl. Phys.* **43** 818-821 (2004).

[4] S. Privitera, C. Bongiorno, E. Rimini, R. Zonca, *Appl. Phys. Lett.* **84**, 4448 (2004).

[5] S. Raoux, C. T. Rettner, J. L. Jordan-Sweet, V. R. Deline, J. B. Philipp, and H.-L. Lung, *2006 European Symposium on Phase Change and Ovonic Science*; available at http://www.epcos.org/library/papers/pdf_2006/pdf_Invited/Raoux.pdf.

[6] C. Peng, L. Cheng, and M. Mansurpir, J. Appl. Phys. **82** (1997).

[7] P. G. Sverdrup, Y. S. Ju, and K. E. Goodson, J. Heat Trans. **123**, 130 (2001).

[8] G. Chen, *Journal of Heat Transfer*, **118**, 539 (1996).

[9] Y. S. Touloukian, R. W. Powell, C. Y. Ho, and P. G. Klemens, Thermophysical Properties of Matter (IFI/Plenum, New York, 1970).

[10] H. J. Ryu, L. J. Klein, M. Asheghi, H. F. Hamann, Proceeding of 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM 2008), 925 (2008).