Methodologies to Study the Scalability and Physics of Phase Change Memory devices

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ABSTRACT

Scalability of Phase Change Memories (PCM) has been the topic of discussion for the last several years. Although the fundamental limitation for the scaling of phase change materials is reported to be of the order of a few nm, it is important to investigate the properties of a PCM device at single digit nm scale. In order to study this, we have developed a number of device structures and fabrication methodologies that are not limited by conventional lithography techniques. One of our approaches is the solution based synthesis of amorphous GeTe nanoparticles that scale down to 1.8nm. In the present work we show that these nanoparticles can fill via holes to fabricate vertical phase change cells that show reasonable switching and cycling characteristics demonstrating for the first time a PCM device based on solution processed nanoparticles. In another approach to scaling, we have explored the use of carbon nanotube as an electrode for PCM cells that enables us to achieve a reset current of 1.4μA which is at least 100 times smaller than the state of the art PCM devices. In addition to the electrode scaling, we have also investigated the thickness scaling of phase change materials using a novel structure called as an Additional Top Electrode (ATE) PCM cell. This structure enables us to directly estimate a key physical parameter, namely the trap-spacing, by applying the Poole-Frenkel model to IV measurements. We report the first direct measurement of the trap spacing in the phase change materials and its dependence on amorphous thickness, reset voltage and drift. We also show how other properties of PCM, such as threshold voltage and noise, scale with thickness. All the projects presented illustrate how novel device structures, nano-materials, and new fabrication methodologies can help extend our understanding of phase change materials and thereby provide better solutions to effectively scale PCM devices to a single digit nm scale.

Key words: phase change, scaling, carbon nanotube, nanoparticle, trap spacing.

1. PCM DEVICE USING SOLUTION PROCESSED GeTe NANOPARTICLES

The major challenge with respect to the scaling of the phase change devices is mainly due to the limitations of the conventional lithography and deposition techniques that make it difficult to scale to the ultimate limit of a few nanometers. One way of overcoming this limitation is by using the bottom-up approach of synthesizing the phase change nanoparticles using solution processing that involves reduced complexity and cost. It has the potential to also enable higher film processing throughput and the ability to deposit the phase change material on a wider range of substrate types and surface topographies. Non-volatile memory can thus be introduced into TFT flexible or large area circuits. Hence the solution-processed methods are much more flexible than the vacuum-based sputtering, CVD, ALD, or thermal evaporation techniques that are currently being used for thin-film deposition of phase change materials. The first demonstration of solution processed chalcogenide thin-film deposition for phase change materials was made by Mitzi et al. [1] using KSB2Sx. Milliron et al. [2] achieved solution-phase deposition of GeSbSe thin films and filled an array of 30nm diameter high aspect ratio vias using them. All of these early works focused only on material synthesis-characterization and did not report device results. Wang et al. [3] fabricated a solution-based SnSe2 phase change film device that had very limited endurance characteristics lasting only up to one or two switching cycles. In a recent work [4], we were able to synthesize size-selective, mono-disperse phase change nanoparticles of diameters ranging from 1.8nm – 3.4nm. These nanoparticles are stable in their amorphous states at room temperature. The method of synthesis and size separation will not be discussed in this paper, but found in [4]. The main focus of this work [5] is to show that these solution processed nanoparticles can be used to make conventional PCRAM (Phase Change Random Access Memory) devices, and that they exhibit the characteristic electrical and phase change properties as that of PCRAM cells fabricated using standard thin film deposition techniques.
The PCRAM devices were fabricated following a conventional lithography technique. The steps involved in the fabrication are shown in Fig. 1a. Our devices range in the dimension from 0.5µm to 10µm. Although the synthesized nanoparticles are only a few nm, we are currently limited by the availability of only a 0.5µm lithography process. However this is only a proof of concept demonstration of the functionality of the solution-processed phase change material and can be scaled down to sub 20nm dimensions with the availability of unconventional patterning techniques based on self-assembled block co-polymer templates [6]. The nanoparticles were drop cast into the vias at selected locations. The scanning electron microscope image of the vias filled with the GeTe nanoparticles (before the deposition of the top electrode) is shown in Fig. 1c. It can be seen that the nanoparticles are well contained within the etched vias. The nanoparticles are then annealed at 80°C to remove all the surrounding ligands and sinter them together. This is essential in-order to have a better contact with the top electrode. The SEM image of the final device after top electrode fabrication is shown in Fig. 1d.

The fabricated devices were first tested by applying a DC sweep voltage across the top and bottom electrode. The results of the sweep are shown in Fig. 2a. It can be seen that with every sweep, the resistance of the cell continuously decreases until it reached a value of about 2 kΩ. This is due to the gradual crystallization of the partially amorphous GeTe nanoparticles. The annealing during the fabrication step did not completely crystallize the nanoparticles. Then write programming was performed on these devices with a 50 ns wide pulse of amplitude 15 V. The cell was then RESET to a value of about 10 kΩ. In the case of SET programming, we use a pulse of smaller amplitude, 3 V and a wider pulse width, 100 us. The SET and RESET pulses were then applied in succession for several cycles. The cell

Figure 1. (a) Process steps involved in fabrication of the PCRAM device with solution processed GeTe nanoparticles. (b) TEM of the size-selected nanoparticles (c) SEM image of the vias uniformly filled with GeTe nanoparticles. (d) SEM image of the final device after top-electrode patterning.

Figure 2. (a) Gradual crystallization of the amorphous Ge-Te nanoparticles by applying DC electrical sweep. (b) Cycling data for the cell between the SET and RESET state. The SET pulse was 3V, 100us and the RESET pulse was 15V, 50ns. (c) SET programming of the PCM device by DC sweep. The cell is repeatedly programmed to the RESET state before each DC SET operation.
was able to switch reliably between the two state for about 150 cycles after which it was stuck in the high resistance state. To our knowledge this is by far the best performing solution-processed PCRAM device reported till date. The endurance data is shown in Fig. 2b. The DC I-V characteristic of the cell was taken after each RESET operation for about 10 cycles. The results are shown in Fig. 2c. The cells show the characteristic threshold switching or ‘snap back’ phenomenon after each cycle. The switching voltage shows a bit of variation from cycle to cycle. This could be because of the quality of the phase change material, material damage caused by cycling, or the poor electrical contact. Overall, this demonstration proves that the phase change materials synthesized by bottom-up approaches can as well exhibit the same characteristics as that of the conventional deposition techniques and can be used to make functional device structures with nanometer-sized dimensions or on flexible substrates.

2. PHASE CHANGE MEMORY WITH CARBON NANOTUBE ELECTRODES

The previous method of nanoparticle synthesis shows that there are no fundamental limitations in terms of the size of the stable phase change materials that can be made. What remains unclear is whether the memory cell device properties at the nanoscale will satisfy the energy and the cell density requirements. In this respect, various CMOS (complementary metal-oxide semiconductor) compatible sub-lithographic sized PCM devices have been demonstrated showing encouraging electrical performance at the nano regime. Further scaling of the PCM device to single-digit nanometer electrode size is recently studied for a lateral PCM cell using carbon nanotubes (CNTs) as the contact electrodes [7]. However, in order to better control the device variation and realize PCM memory array with high device density, the electrical breakdown process for each individual device that is required to create the gap in a lateral CNT for a PCM cell must be avoided. The conventional vertical PCM structure resolves this difficulty and consumes a smaller device area. Moreover, the cross-point architecture for vertical memory structure combines the advantage of the highest device density and ultimate scaling potential, and is thereby widely regarded as the most appealing concept for the next generation NVM. In this work [8], we demonstrate a fully functional cross-point PCM cell with 1.4μA Ireset. We utilize CNTs as the bottom electrode for the memory cell, which effectively confines the active device area down to nanometer regime and contributes to the substantial reduction of Ireset by two orders of magnitude and energy by over 10× as compared to the state-of-the-art.

The main process flow of the vertical cross-point PCM cell with CNT bottom electrode is illustrated in Fig. 3a. Horizontally-aligned CNTs (Fig. 3b) are grown in methane (CH4) and hydrogen (H2) and transferred onto SiO2/Si substrate to form the bottom electrode. The mean diameter of the aligned CNT is 1.2nm±0.3nm as measured by AFM. Pd is then e-beam evaporated as the contact metal pad for CNTs with a separation of 4μm. The distribution of the CNT resistance between two Pd metal pads (including the contact resistance) at the low voltage is shown in Fig. 3c. Unwanted CNTs outside the device area are etched away by O2 plasma, leaving 2-4 CNTs/ cell on average. After that, 10nm GST is deposited by DC sputtering on top of CNTs, followed by the patterning of the top Pt electrode using lift-off. A thin 2nm Al2O3 is sputtered in the end to passivate the GST material. Fig. 3d shows the scanning electron microscopy (SEM) image of the fabricated PCM cell.

![Figure 3](image-url)

Figure 3: (a) Main process flow of the cross-point PCM cell (b) SEM image of the horizontally-aligned CNTs. (c) Resistance distribution of CNTs between Pd metal pads. Contact resistance is included (d) False-colored SEM image of the cross-point PCM cell with CNT bottom electrode (BE) covered by GST and Pt top electrode (TE).
Contrary to the conventional PCM devices whose initial states are in the crystalline or low resistance states, the PCM cell in this work is in the as-deposited amorphous state and has a high resistance value (~60-70 MΩ) to begin with. Starting from the high-resistance amorphous state, we apply a DC current sweep to set the cell. As the voltage building up across the a-GST exceeds the threshold value (V_{th}), crystalline paths form through the a-GST layer and the device sets from a high resistance off-state to a low resistance on-state (Fig. 4a). For the reset process, we apply 50 ns reset pulse with sharp falling edge (10 ns) to melt-quench the cell. To study the switching mechanism, we perform the 3D finite element simulation using COMSOL and plot the temperature profile at the Pt/GST/CNT cross-section to confirm the temperature rise within the GST due to the current flowing through the CNT electrodes as shown in Fig. 4b. From Fig. 4b, we observe the temperature profile is confined within a narrow region and the highest temperature region is localized on top of CNTs, which implies the crystalline paths are only partially amorphized during the subsequent reset process. As a result, the thickness of the formed amorphous region is much reduced from the initial 10nm value. As V_{th} decreases linearly with the thickness of the amorphous region following the constant threshold field scaling of phase change materials, the PCM cell stabilizes at a much lower V_{th} for the 60th and 100th cycles, as shown in Fig. 4a. Fig. 4c shows the set programming current (I_{set}) distribution and V_{th} distribution of the vertical PCM cell. The mean value of I_{set} is as low as ~0.5 μA, two orders of magnitude lower than the PCM devices using conventional metal electrodes. It is worth mentioning that the DC programming in the set process here is used only for the purpose of illustrating the threshold switching I-V characteristics of the cell for different cycles. In practical applications, pulse programming is used to switch the cell to the low-resistance set state.

The CNT/PCM device successfully switches for over 100 cycles, maintaining a 10x resistance ratio, as shown in Fig. 5a. Fig. 5b shows cycle to cycle resistance distribution at low-resistance on-state (R_{on}) and high-resistance off-state (R_{off}). Good read-disturb immunity is also achieved for a constant voltage stress of 1V, which corresponds to 10^{11} endurance cycles of 100ns read pulses (Fig. 5c). It must be noted that the R_{off} here is ~20 MΩ, which is smaller than the initial value (60-70 MΩ) of the cell at the as-deposited amorphous state. This confirms again that only a portion of the crystalline conductive path is amorphized where the temperature is highest (see Fig. 4b). Hence R_{off} is smaller than its initial value when the entire cell is in the as-deposited amorphous state.
To study the energy consumption of the cross-point PCM cell, $I_{\text{reset}}$, which is one of the most critical parameters that sets the lower bound for energy consumption for PCM, is measured with the measurement setup illustrated in Fig. 6a. The current flowing through the PCM cell is calculated by dividing the sensed voltage of the active probe by its $10\,\text{M}\Omega$ input series resistance. Fig. 6b shows the typical phase transition characteristics (R-I curve) of the PCM cell. Because of the Joule heating required to melt-quench the phase change material, the $I_{\text{reset}}$ scales with the area of the bottom contact electrode as large collection of literature data and the ITRS[9] projection shows (see Fig. 7a). With the effective confinement of conducting GST path down to the scale of the CNT diameter by the bottom CNT electrode, a remarkable reduction of $I_{\text{reset}}$ down to $1.4\,\mu\text{A}$ (a milestone in the published data, and is ~5× smaller than the $I_{\text{reset}}$ of lateral PCM cells with CNT electrode [7]) is achieved, corresponding to an effective contact area of ~2.54 nm$^2$ following the linear scaling trend to approach its ultimate limit projected from a large body of experimental data [10] shown in Fig. 7a. But it is also worth mentioning that this linear scaling of the $I_{\text{reset}}$ with contact area may not hold when the devices are small (e.g. the thermal environment may be different). Therefore the effective contact area quoted above is only an estimate that needs to be further verified. The write energy per bit of the device is as low as $210\,\text{fJ}$ using a 10 ns reset pulse with 4.5 ns falling edge. This is over $10^3×$ smaller than the state-of-the-art PCM devices (Fig. 7a). The performance comparison between this work and other state-of-the-art PCM devices is summarized in Table 1. It can be clearly seen from the table that PCM shows very good scaling trend in terms of the $I_{\text{reset}}$ and hence are suitable for very high density memory arrays. With the use of CNT electrodes, we have shown that PCM can be highly scaled both in terms of area and energy that makes them highly suitable for ultra high density, very low power embedded memory applications.

Figure 6. (a) Measurement setup for reset current measurement (b) phase transition (R-I curve) of PCM cells with an ultra low $I_{\text{reset}}$ of 1.4µA. Different colors are used to correlate the set state (blue) and reset (red) state of the memory cell.

Figure 7. (a) Scaling trend of $I_{\text{reset}}$ vs. contact diameter. There is a large gap between the $I_{\text{reset}}$ current density required and the memory cell selector current drive capacity. A record-low 1.4µA $I_{\text{reset}}$ and 210 fJ/bit write energy is achieved in this work. (b) Performance comparison of various PCM devices
3. DIRECT MEASUREMENT OF TRAP SPACING USING ADDITIONAL TOP ELECTRODE DEVICES

The earlier work on nanoparticle synthesis and carbon nanotube electrode based PCM addresses the aspect of the ultimate scaling limit of the phase change memory devices. However, there are a number of challenges that are to be addressed in terms of understanding the physics of the conduction mechanism in the phase change material and how it is impacted by material scaling. For this purpose, we modified the standard mushroom PCM cell by inserting an additional metal layer in the phase change layer. We call this structure as Additional Top Electrode (ATE) device [11]. One of the key advantages of this structure is the confinement of the amorphous region thickness to a well-defined value. This enables us to directly estimate a key physical parameter, namely the trap-spacing, by applying the Poole-Frenkel model to IV measurements. We report the first direct measurement of the trap spacing in the phase change materials and its dependence on amorphous thickness, reset voltage, and drift [12].

The structure resembles that of a standard mushroom PCM cell except for a thin, electrically floating, metal (tungsten) layer called the Additional Top Electrode (ATE) that is buried inside the phase change layer as shown in Fig. 8a. This ATE layer confines the amorphous region to a well-defined thickness when the cell is programmed in the reset state. The total thickness of the phase change layer (GST1 + GST2) is kept constant (100 nm). By varying the height of the ATE layer from the heater-GST interface, we can achieve amorphous regions in GST1 of varying thicknesses. The GST2 layer provides very good heat confinement causing the GST1 layer to amorphize completely. The TEM cross-section of a 20nm ATE device after programming the cell in the fully amorphous state is shown in Fig. 8b. We can see that the amorphous region covers the entire region of GST1 that is above the heater and also forms a dome-shaped region on top of the ATE layer. This is because of the high thermal conductivity of the W layer that is used for the ATE. Finite element simulations were performed on a cell with a GST1 thickness of 20nm. Fig. 8c shows the temperature profile in the fully reset state where the GST1 layer is completely melted (T > 900K) and amorphized and a similar dome-shaped area on the top of the ATE as seen in the TEM cross-section. Similar programming is achieved for the other ATE devices of different thicknesses. Fig. 8d shows the temperature profile along the center of the cell for different GST thicknesses. It can be seen that for higher reset voltages, the amorphous region extends further over top of the ATE layer. However, this is not an issue because when the cell is being read, the current flows through the heater, the confined GST1 amorphous layer, laterally spreading through the ATE layer (as the amorphous GST on top is highly resistive) and then through the crystalline GST region on top. The current path is marked by yellow arrows in the Fig. 8a. The ATE devices are programmed by applying a reset pulse of width 50ns between the top electrode (TiN) and the bottom electrode (W). The amplitude of the reset pulse is increased continuously and the programmed resistance is measured after each pulse. When the measured resistance reaches a saturation value, then the device is said to be completely programmed or in other words, the region below the ATE layer is completely amorphized. Fig. 9a shows the saturation of the reset resistance for ATE devices of different thicknesses. The resistance saturation occurs for nearly the same reset voltage of 6.5V for all ATE thicknesses. The fully programmed reset resistance increases with increasing amorphous GST1 thickness and shows a
linear trend as shown in Fig. 9b. The measured threshold voltages for each of these thicknesses also show a linear trend. The critical threshold field extracted from the slope of this line is about 0.14MV/cm.

Figure 9. (a) RESET programming of ATE devices of different thicknesses (b) Measured peak resistance and threshold voltage for different thicknesses. (c) Sub-threshold IV characteristics for the fully programmed ATE devices and the method of extraction of trap spacing (d) Extracted trap spacing for different thicknesses and the average number of hops in the conduction path. (e) The normalized noise spectral density for a fully programmed 40 nm ATE device showing exponential noise behavior for increasing bias (f) The scaling of the normalized noise with GST thickness.

The trap spacing of the amorphous region can be extracted by measuring the sub-threshold slope of the IV-characteristics based on the trap assisted conduction model proposed in [13]. All the devices are programmed in their maximum reset resistance state. The current-voltage characteristics of the various ATE devices are shown in Fig. 9c. The sub-threshold slope is extracted from the exponential region of the I-V curve. Since the thickness of the amorphous region is known for these devices, we can then directly extract the trap spacing based on the Poole-Frenkel model described in [13]. The values of the extracted trap spacing for the various thicknesses are shown in Fig. 9d. It can be seen that the average trap spacing decreases with the thickness of the amorphous region. This is a newly observed phenomenon as the trap spacing is generally considered to be constant, independent of the amorphous thickness for the models proposed so far [13]. Hence it is important to include this change in the trap spacing when modeling the I-V characteristics of the intermediate states of the standard PCM cells. It is also important to note that, the average number of hops made by carriers as they travel through the amorphous layer, which is given by the amorphous thickness divided by the trap spacing, gradually increases with the thickness as shown in Fig. 9d. The smallest thickness of 8nm has on an average only one hopping event in the entire GST thickness. The implications of this can be clearly seen in the noise measurements in these devices. PCM cell with ATE of 40nm was programmed to it’s fully reset state. The 1/f noise was then measured at various bias values of the sub-threshold region. The power spectral density of the current noise for various bias values of the sub-threshold region. The power spectral density of the current noise for various bias values is shown in Fig. 9e. It can be clearly seen that the noise spectral density follows a 1/f trend in the low frequency regime. Also the spectral density is exponentially dependent on the bias voltage showing that the 1/f noise is an indicator of the current generation process in the amorphous material which in this case is believed to follow Poole-Frenkel mechanism. The 1/f noise measurement was then performed on the ATE devices of different thicknesses. The normalized spectral densities of current noise for the different amorphous thicknesses are plotted in Fig. 9f. We can see that the noise is higher for smaller amorphous thicknesses. This can be explained based on the trap spacing results that was observed earlier (Fig. 9d). The average number of traps that the carrier has to hop through is larger for a thicker GST device. This means that there is a large averaging effect of the noise along the path [14]. Hence the noise is much higher for smaller thicknesses where this
averaging effect is minimized. This effect shows that the PCM noise would be a major concern as we scale the device dimensions.

CONCLUSION
We discussed some of the methodologies that are used to investigate the scalability and physics of phase change memory devices. The solution processing of the nanoparticles has enabled us to synthesize stable amorphous nanoparticles down to 1.8nm, that was used to make a functional PCM device. This is the first demonstration of the PCM device using solution processed nanoparticles. Future work involves the filling of highly scaled via holes to make devices with better endurance. The use of carbon-nanotube as the electrode has enabled us to demonstrate a fully functional PCM device at single-digit nm dimension. The memory cells show encouraging properties such as a dramatic reduction of the reset programming current ($I_{\text{reset}}$) down to 1.4 µA (smallest value ever reported), 210 fJ write energy, stable switching characteristics and decent resistance distribution. To further reduce the programming energy and improve the device performance, further studies on the contact resistance (CNT/metal and CNT/GST), reliability, and the electrothermal property of CNTs are needed. Finally, the Additional Top Electrode structure has enabled us to directly measure the trap spacing of the amorphous region and correlate the results with the measured 1/f noise. The results give valuable insight into the nature of traps and the conduction mechanism in the amorphous GST.

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Biographies

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