Fabrication and Characterization of Chalcogenide-based Non Volatile Memory Devices on Flexible Substrate

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1. Introduction

Chalcogenide materials are used for their application in either phase change memories (PCM) or conductive-bridge random access memories (CBRAM). While PCM concept relies on the reversible amorphous-crystalline phase transition of the chalcogenide layer with a concomitant resistance change [1-3], CBRAM devices exploit the chalcogenide material as a solid electrolyte in which conductive filaments are formed or dissolved thanks to redox reactions at electrodes [4].

The aim of this work is to study the well-known chalcogenide $Ge_2Sb_2Te_5$ (GST) material to fabricate small density crossbar arrays of non-volatile memory cells on flexible substrates for future Radio Frequency Identification (RFID) applications such as "smart-tags". To reach this goal, an original heterogeneous process combining inkjet printing and RF sputtering deposition methods was developed. The amorphous-to-crystalline phase transition was studied using a combination of three *in situ* characterization techniques during thermal annealing while CBRAM electrical switching was studied by using Conductive-Atomic Force Microscopy (C-AFM). It is shown that GST layer exhibits a versatile behavior enabling both PCM and CBRAM concepts on flexible substrates.

2. Experiments

2.1 Sample preparation: a heterogeneous process

Silver lines (350 nm-thick, 100 µm wide) were deposited on 120 µm-thick polyimide (Kapton® 500-HN) foils by inkjet printing of commercial silver ink embedding Ag nanoparticles. The samples were then annealed during 30 min at 200°C in order to eliminate the organic solvent and favor the coalescence of silver nanoparticles. $Ge_2Sb_2Te_5$ thin films (35 nm) were subsequently deposited through a shadow mask by radiofrequency (RF) magnetron sputtering from a high purity (99.9999%) stoichiometric target. Few samples were finally covered by an inert counter top electrode, consisting of W lines (200 nm thick, 100 µm wide) deposited by RF-magnetron sputtering through a shadow mask perpendicularly to silver lines to produce crossbar devices (Fig. 1). Besides, GST layer was also deposited on SiO_2/Si substrate for physical characterization.

2.2 Combined in situ structural and electrical characterization

Simultaneous *in situ* x-ray diffraction (XRD), x-ray reflectivity (XRR) and sheet resistance (Rs) measurements were performed on the BM05 beamline at ESRF (Grenoble, France) using a dedicated vacuum chamber (10^{-6} mbar), equipped with a heating stage and a 4-point probes sheet resistance set-up. XRD, XRR and Rs measurements were simultaneously performed during GST layer annealing with a constant heating rate of 2°C/min, from room temperature up to 320°C.

2.3 Ex-situ electrical and topographic AFM characterizations

The resistance switching of the memory stack (*i.e.* GST/Ag) was deeply investigated at nanoscale by means of C-AFM on samples without a top electrode. Local current-voltage characteristics were measured by applying a voltage bias to the bottom electrode, the AFM tip being grounded. In complement, individual memory elements defined by the 100×100 μm^2 cross-point area between perpendicular Ag (bottom electrode) and W (top electrode) lines were also electrically characterized in ambient conditions using an HP 4156C analyzer (Agilent Company).

3. Results and discussion

PCM behavior of GST layer was studied by an original experimental setup combining *in situ* characterization techniques performed simultaneously during thermal annealing [5]. These combined

experiments (XRD, XRR and Rs) unambiguously demonstrated concomitant changes in structural and electrical properties while $Ge_2Sb_2Te_5$ film was heated. Indeed, around 152°C GST layer (35 nm thick) undergone a transition from its as-deposited amorphous form towards a cubic metastable f.c.c. crystalline phase. The crystallization process was accompanied by a density increase, an associated contraction in the film thickness and a switch from a high to a low resistance (Fig. 2). In the case of 35 nm thick GST films, a peculiar two-layers microstructure consisting of a polycrystalline layer capped by an amorphous one was observed after the experiments. The persistence of the amorphous phase was discussed on the basis of various hypotheses such as the lack of pre-existing nucleation sites at the free surface, oxidation and/or a phase separation that may occur during heating and crystallization. The influence of the GST layer thickness on the transition temperature is being studied.

GST layer used as solid electrolyte for CBRAM applications on flexible substrate was characterized by C-AFM [6]. First, a resistive switching at nanoscale on GST/Ag/SiO_2/Si stack was observed: while applying voltage sweeps in a range -1.0 V and +1.0 V to the bottom electrode, a neat hysteresis loop was observed on the current-voltage characteristics (Fig. 3). This loop features the creation (set) and dissolution (reset) of conductive filaments formed by the electro-deposition of silver-rich aggregates underneath the AFM tip within the GST layer. Besides, sequential set/reset operations achieved during C-AFM measurements revealed that the resistance switching is accompanied by the reversible formation of a conductive hillock underneath the AFM tip. This memory effect was also evidenced at a micrometric-scale by means of nano-lithography as well as on individual crossbar memory elements fabricated on a plastic foil and featuring a tungsten top electrode.

4. Conclusion

GST layers were studied for both PCM and CBRAM applications. For PCM applications, simultaneous *in situ* synchrotron techniques (x-ray diffraction and reflectivity) and sheet resistance measurements were advantageously combined to evidence correlated changes in structural and electrical properties. Regarding CBRAM application, a reproducible memory effect was successfully demonstrated on flexible substrate at nanometric scale by using C-AFM. The resistance switching mechanisms were interpreted in terms of electrodeposition/dissolution of silver-rich conductive filaments within the GST layer. The next steps will consist in (i) exploiting a possible interplay between CBRAM and PCM effects; (ii) evaluating the electrical performances of single memory devices (*i.e.* cycling, retention…); (iii) assessing the impact of mechanical stress (bending) on the electrical characteristics; and (iv) engineering GST layers with suited density and thickness.

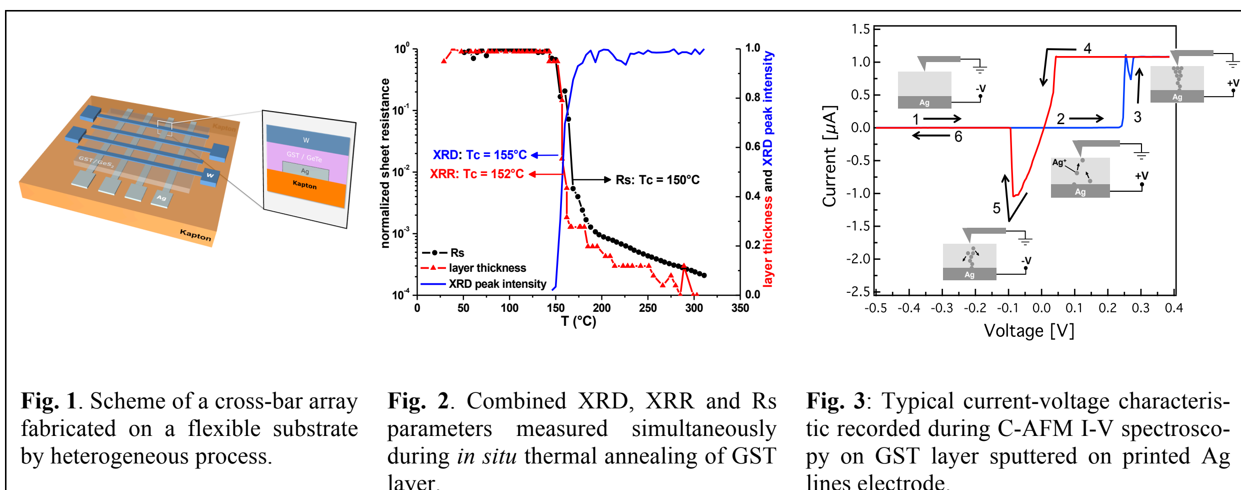

Fig. 1. Scheme of a cross-bar array fabricated on a flexible substrate by heterogeneous process.

Fig. 2. Combined XRD, XRR and Rs parameters measured simultaneously during *in situ* thermal annealing of GST layer.

Fig. 3: Typical current-voltage characteristic recorded during C-AFM I-V spectroscopy on GST layer sputtered on printed Ag lines electrode.

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